Customer No.: 31561
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Application No.: 10/708,489

AMENDMENT

To the Claims:

Claim 1 (previously presented) A voltage regulator apparatus, comprising:

a voltage regulator having an output terminal to provide an output voltage regulated according to a reference voltage;

a first transistor having a first terminal coupled to a positive terminal of a voltage source, a second terminal coupled to a first bias, and a third terminal directly coupled to the output terminal of the voltage regulator; and

a second transistor having a first terminal coupled to the third terminal of the first transistor, a second terminal coupled to a second bias, and a third terminal coupled to a negative terminal of the voltage source.

Claim 2 (original) The voltage regulator apparatus as recited in claim 1, wherein the voltage regulator comprises:

an error amplifier having a positive input terminal, a negative input terminal, and an output terminal, wherein the negative input terminal is for receiving the reference voltage;

a third transistor having a first terminal coupled to the positive terminal of the voltage source, a second terminal coupled to the output terminal of the error amplifier, and a third terminal outputting the regulated output voltage; and

a load circuit used to divide the regulated output voltage, and provide a feedback voltage to the positive terminal of the error amplifier.

Claim 3 (original) The voltage regulator apparatus as recited in claim 2, wherein the third transistor is a PMOS transistor.

Claim 4 (original) The voltage regulator apparatus as recited in claim 2, wherein the load circuit comprises:

a first resistor having a first terminal to receive the regulated output voltage, and a second terminal to output the feedback voltage to the positive terminal of the error amplifier; and

a second resistor having a first terminal coupled to the second terminal of the first resistor, and a second terminal coupled to the negative terminal of the voltage source.

Claim 5 (original) The voltage regulator apparatus as recited in claim 1, wherein the first transistor is an NMOS transistor.

Claim 6 (original) The voltage regulator apparatus as recited in claim 1, wherein the second transistor is a PMOS transistor.

Claims 7 and 8 (canceled)

Claim 9 (New) A voltage regulator apparatus, comprising:

a voltage regulator having an output terminal to provide an output voltage regulated according to a reference voltage, the voltage regulator comprising an error amplifier for receiving the reference voltage;

a first transistor having a first terminal coupled to a positive terminal of a voltage source, a second terminal coupled to a first bias, and a third terminal directly coupled to the output terminal of the voltage regulator; and

a second transistor having a first terminal coupled to the third terminal of the first transistor, a second terminal coupled to a second bias, and a third terminal coupled to a negative terminal of the voltage source.

Claim 10 (New) The voltage regulator apparatus as recited in claim 9, wherein the error amplifier of the voltage regulator having a positive input terminal, a negative input terminal, and an output terminal, the negative input terminal being for receiving the reference voltage.

Claim 11 (New) The voltage regulator apparatus as recited in claim 10, wherein the voltage regulator further comprises:

a third transistor having a first terminal coupled to the positive terminal of the voltage source, a second terminal coupled to the output terminal of the error amplifier, and a third terminal outputting the regulated output voltage; and

a load circuit used to divide the regulated output voltage, and provide a feedback voltage to the positive terminal of the error amplifier.

Claim 12 (New) The voltage regulator apparatus as recited in claim 11, wherein the third transistor is a PMOS transistor.

Claim 13 (New) The voltage regulator apparatus as recited in claim 11, wherein the load circuit comprises:

a first resistor having a first terminal to receive the regulated output voltage, and a second terminal to output the feedback voltage to the positive terminal of the error amplifier; and

a second resistor having a first terminal coupled to the second terminal of the first resistor, and a second terminal coupled to the negative terminal of the voltage source.

Claim 14 (New) The voltage regulator apparatus as recited in claim 9, wherein the first transistor is an NMOS transistor.

Claim 15 (New) The voltage regulator apparatus as recited in claim 9, wherein the second transistor is a PMOS transistor.